REMARKS

This application has been carefully reviewed in light of the Office Action dated January 19, 2005. Claims 1 to 13 are pending in the application, of which Claims 1, 4 and 7 to 13 are independent. Reconsideration and further examination are respectfully requested.

The title was objected to as not being descriptive. The Examiner suggested a new title which has been adopted herein. Accordingly, withdrawal of the objection to the title is respectfully requested.

Claims 1, 4 and 7 to 13 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the term "rotation/reversal" was considered indefinite. Claims 1, 4 and 7 to 13 have therefore been amended to read -- rotation and/or reversal --. Accordingly, withdrawal of these rejections is respectfully requested.

Claims 1 to 8, 11 and 12 were rejected under 35 U.S.C. § 102(b) over U.S. Patent No. 4,929,085 (Kajihara). Claims 9, 10 and 13 were rejected under 35 U.S.C. § 103(a) over Kajihara in view of U.S. Patent No. 5,563,625 (Scott). Reconsideration and withdrawal of these rejections are respectfully requested.

Turning to specific claim language, amended independent Claim 1 is directed to an image processing method which includes a numerical signal generation step of sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal, a bit conversion step of generating and outputting, from the output signal in said numerical signal generation step being managed as an input signal, a signal that order of bits in the input signal has been exchanged or a signal that value of bit in the input signal has been reversed, and a control step of controlling the bit order exchange operation or the bit value reversal operation in

said bit conversion step. Image data divided into pixel data and one-dimensionally arranged and stored in a memory is read and output in synchronism with the sequential operation in the numerical signal generation step, and the output signal generated in the bit conversion step is read and output as an address signal, so that a rotation and/or reversal process to a former image is performed.

In contrast, Kajihara discloses bit-shifting of already held n-word data according to clock synchronization and selectively outputting the bit data in order to select and output data converted by a rotation (either vertical or horizontal conversion) circuit. That is, the input image data itself is the target of the conversion process and is selected and output. This process is not the same as Applicant's use of numerical signals the are sequentially generated. In Claim 1, the binary numerical signal treated is not the image data itself but is the signal to be used to control rotation and reversing of the image data. By generating the binary numerical signals, it is possible to downsize the scale of a circuit to achieve high-speed operation.

In addition, Claim 1 includes the feature of "generating and outputting, from the output signal in said numerical signal generation step being managed as an input signal, a signal that order of bits in the input signal has been exchanged or a signal that value of bit in the input signal has been reversed" whereby the order of bits of the data output in the numerical signal generation step is exchanged or the bit value is reversed, and the exchanged or reversed data is output. Accordingly, exchanging of the order of bits results in bit rearrangement and reversing the bits results in reversing of the value of binary number (i.e., "0" ↔ "1").

However, in Kajihara, the bit which is reversed by the bit-order reversing circuit is the bit which constitutes the image data. That is, Kajihara discloses that the bit value, which is the image data itself, is reversed, but does not disclose that the bit arrangement of the binary

numerical signal (not image data) is exchanged and the value of the binary numerical signal is reversed.

Furthermore, in accordance with Claim 1, the image data is divided into pixel data and one-dimensionally arranged and stored in a memory. The data is read and output in synchronism with the sequential operation of the numerical signal generation step while the output signal is read and output as an address signal, so that a rotation and/or reversal process to a former image is performed. Therefore, the output of the binary numerical signal processed in the bit conversion step is used as the address for reading the image data stored in the memory.

In contrast, Kajihara discloses that the order of writing access and reading access is controlled based on the transfer mode and the rotation mode, but does not disclose any process corresponding to Applicant's bit conversion step. Thus, Kajihara neither discloses nor suggests that the output of the binary numerical signal processed in Applicant's bit conversion step is used as the address for reading the image data.

In light of the deficiencies of Kajihara as discussed above, Applicant submits that Claim 1 is now in condition for allowance and respectfully requests same. Claim 4 and Claim 9 are directed to a method and a storage medium, respectively, in accordance with the apparatus of Claim 1. Therefore, Applicant submits that Claim 4 and Claim 9 are also in condition for allowance and respectfully requests same.

Turning now to Claim 7, Claim 7 is directed to an image processing method. As in Claim 1, the method of Claim 7 includes a numerical signal generation step of sequentially generating and outputting regular binary numerical signals in synchronism with a clock signal, a bit conversion step of generating and outputting, from the output signal in said numerical signal generation step being managed as an input signal, a signal that order of bits in the input signal

has been exchanged or a signal that value of bit in the input signal has been reversed, and a control step of controlling the bit order exchange operation or the bit reversal operation in said bit conversion step. However, Claim 7 includes the feature that the image data is written in a memory in synchronism with the sequential operation in said numerical signal generation step by using the output signal generated in said bit conversion step as an address signal, and the image data written in the memory is read according to addresses of predetermined order, so that a rotation and/or reversal process to a former image is performed.

As Claim 7 includes the data conversion and memory addressing features of Claim 1, Applicant submits that the discussion from above in regard to Claim 1 applies equally to Claim 7. Accordingly, Applicant submits that Claim 7 is also in condition for allowance and respectfully requests same.

Claim 8 and Claim 10 are directed to an apparatus and a storage medium, respectively, in accordance with the method of Claim 7. Therefore, Applicant submits that Claim 8 and Claim 10 are also in condition for allowance and respectfully requests same.

Claim 11 is directed to an image processing method. The method includes an input step of inputting a block image and positional information of the block image, an image rotation and/or reversal processing step of rotating or reversing the input block image by a block, and outputting the rotated or reversed block image and a conversion step of converting the positional information of the input block image into the positional information of the image after the rotation or the reversal. The method further includes the feature that the conversion in said conversion step is a process corresponding to the content of the image rotation or the image reversal in said image rotation and/or reversal processing step, and in the conversion, the positional information for the entire image before the rotation or the reversal where the block

image stands is converted into the positional information for the entire image after the image rotation or the image reversal in said image rotation and/or reversal processing step, and the converted positional information is added to the rotated or reversed block image and output.

In contrast, Kajihara does not disclose that a block image and the position information thereof are input. As such, Kajihara cannot disclose converting the positional information of the input block image into the positional information of the image after the rotation or the reversal. Instead, Kajihara discloses reading the specific memory address of the image data stored in the memory and convert the read-out image. That is, the target of the conversion in Kajihara is the image data itself. This is not the same as processing the positional information of the block image as featured in Claim 11.

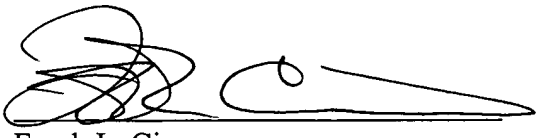
In light of the deficiencies of Kajihara as discussed above, Applicant submits that Claim 11 is now in condition for allowance and respectfully requests same. Claim 12 and Claim 13 are directed to a method and a storage medium, respectively, in accordance with the method of Claim 11. Therefore, Applicant submits that Claim 12 and Claim 13 are also in condition for allowance and respectfully requests same.

The other pending claims in this application are each dependent from the independent claims discussed above and are therefore believed allowable for at least the same reasons. However, individual consideration of each dependent claim on its own merits is respectfully requested as each dependent claim is also deemed to define an additional aspect of the invention.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicant's undersigned attorney may be reached in our Costa Mesa, CA office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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